Control Strategy of Automatic Gear Shift for Hybrid Electric Machinery Vehicles

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Abstract: Automatic transmission control strategy is the key to measuring whether the vehicle can play its power, economy and driving ability after adopting automatic transmission technology. Therefore, it is the core technology of automatic mechanical transmission (AMT) and the research hotspot of automobile automatic transmission technology in China. Its main research contents include: optimal power shift control strategy and optimal energy consumption economy shift control strategy. In this paper, the AMT of a pure electric bus is taken as the research background, with the help of ATLAB/SIMULINK software, the simulation modeling method is used to improve the optimal power shift control strategy algorithm of the existing electric bus, and a more precise shift surface is obtained. Aiming at the optimal motor efficiency, a two-parameter shift control strategy is proposed based on the existing two-parameter shift control strategy. Three-parameter optimal economic shift control strategy and the optimal shift surface are obtained by simulation modeling algorithm. In order to comprehensively consider the dynamic and economic requirements of driving vehicles, a control scheme of automatic switching between dynamic shift and economic shift mode is formulated, and the above-mentioned shift strategy is implemented. The feasibility and superiority of these methods are verified by experiments.

1. Introduction

Automotive steering system is the key factor to improve the handling stability of the vehicle and to reduce the driver's controlling load and to improve the performance of the Driver-vehicle Closed-loop System. According to the steering power source, the steering system can be divided into mechanical steering system and power steering system [1]. In mechanical steering system, we take the driver's physical power as power source. Besides, we use mechanical transmission components, but due to the small output of the steering torque, the scope of application should be limited. Power steering system, based on the mechanical steering system, it added a steering power assisting device. Therefore, it takes the driver physical strength and the power of the motor as steering power source. According to the different ways of providing power, we could divide the systems into Hydraulic Power Steering, namely HPS, Electronically Hydraulic Power Steering System, namely EHPS, Electric Power Steering, namely EPS and Steer-by-Wire, namely SBW.

2. Phase Deviation State Diagram

In the description of clock synchronization state diagram, we usually adopt the transmission delay description method[9], namely use the transmission delay of the time stamp between two nodes to form the edge of the clock synchronization state diagram. However, with the development of modern network technology and the expansion of the scope of the clock synchronization, the information transmission appears to be sudden and intermittent, so it is difficult for us to accurately estimate the time stamp of the transmission delay. Due to the fact that the clock drift rate is more stable than the transmission delay of time stamp, we take the phase deviation as the basis of generating state diagram. The application of continuous time interval is more accurate than real-time interval, and it could conduct real-time and dynamic evaluation on the performance of clock synchronization. Besides, the application of continuous time interval could determine the

system stability by exchanging the information of phase deviation state diagram, so as to improve the accuracy of clock synchronization in the network.

As shown in Figure 1, we assume that that the nodes i, j, k, l are the synchronization nodes in the FlexRay network. We establish the phase offset trend equation $y = P \times x + C$ by the least square method. In this equation, x stands for phase deviation, weight P stands for change rate of x, namely the node's clock drift rate.
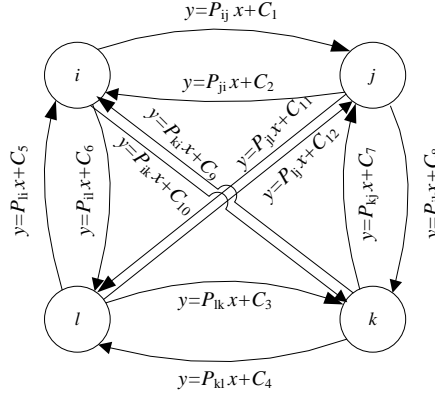

Fig. 1. Phase deviation state diagram

If the weights between synchronization nodes i and j meet the equation $P_{ij} = -P_{ji}$ (the weight P_{ij} is the j clock drift rate when i is taken as reference node), namely $|P_{ij}| = |P_{ji}|$, which means the clock drift rate of node i equals to that of node j, and the clock synchronization of the two nodes are stable, and through continuous clock correction the phase deviation can be synchronously reduced. Therefore, when there is no synchronization node error in the network, the whole phase deviation state diagram will be stable. If there is an exception in the clock synchronization nodes, then the weight values in the figure that take the node as the starting point and the end point will be changed.

3. The Dynamic Detection Method Synchronous Node

There are at least three synchronization nodes in the FlexRay network, and each synchronization node sends or receives the synchronization frame in static segment (namely the ST segment). Under normal circumstances, if there is a synchronization node error, we should use the method of dealing with non synchronous node to deal with it, namely through judging the value and count value of the error cycle of zSyncCalcResul to make the node from being POC: normal active state to the POC: passive state or POC: halt state. If the synchronization node enters the normal POC: normal state, then it is forbidden to send the synchronization frame, but it still could receive the frame; if the synchronization node enters the POC: halt state, then we should re initialize the node. Although the synchronization error could not paralyze the clock synchronization of the entire network, it still affects the accuracy of the clock synchronization. In order to reduce this kind of influence, by exchanging the information of the phase deviation state diagram, we should conduct active detection towards the synchronous nodes and evaluate the stability of the network, thus to improving the accuracy of the clock synchronization.

Table 1 Transmission time slot and content of the synchronization frame

NODE	i	j	k	l
Synchronous frame transmission time slot	slot1	slot2	slot3	slot4
Transmitted content of the synchronization frame	Pji,Pki,Pli	Pij,Pkj,Plj	Pik,Pjk,Plk	Pil,Pjl,Pkl
Received content of the synchronization frame	Pij,Pik,Pil	Pji,Pjk,Pjl	Pki,Pkj,Pkl	Pli,Plj,Plk

Take FlexRay network in Figure 1 as an example, and table 1 shows the synchronous frame transmission time slot and the content in the load period.

For synchronous node i, after received the synchronous frames sent by other nodes, it should read related phase deviation's state diagram weights Pij,Pik,Pil from load segments, and then compare with weights Pji,Pki,Pli obtained from this node to detect the stability of the FlexRay network. If all synchronization nodes have been in a synchronous correction state, then we can take the weights Pji',Pki',Pli' calculated out in pre cycle to detect the clock synchronization performance of this node i.

$Error1 = |P_{ji} - (-P_{ij})| + |P_{ki} - (-P_{ik})| + |P_{li} - (-P_{il})| = |P_{ji} + P_{ij}| + |P_{ki} + P_{ik}| + |P_{li} + P_{il}|$ is used to evaluate the clock synchronization state between node i and other nodes, and this equation is a general measure of the network stability. If the error is equal to 0, which signifies that the synchronization clock correction between the node i and other nodes maintains a synchronized stable state; if the error is greater than limitpassive1, which signifies that node i deviates from the clock synchronization range of the network, then the node should enter the POC: normal passive state; if the error is greater than limithalt1, which signifies that the normal clock synchronization between node i and other synchronization nodes can't be maintained, thus we should initialize the node. Since the number of MT in the communication cycle is constant, that is to say FlexRay could achieve synchronization when the clock synchronization layer is the maximum one. Therefore, so when the clock deviation maintains a MT, the node must enter the POC: halt state. Taking into account that Error1 is obtained from the absolute value, then we can define the limit values in the conditions that the nodes enter the POC: halt state and POC: normal passive state respectively as

$$limithalt1 = 2 \times pMicroPerMacNom \quad (1)$$

$$limitpassive1 = 0.5 \times limithalt1 \quad (2)$$

From the two equations, we can know that pMicroPerMacNom is the number of μT in one MT. The new frequency correction value could be obtained from the FTM algorithm, namely,

$$dynratecor1 = FTM(P_{ji}, P_{ki}, P_{li}) \quad (3)$$

Pji,Pki,Pli are the phase deviation change rates when we take j,k,l as the reference nodes. Due to the face that these weight values are based on the phase deviation change rates of multiple cycles, so $dynratecor1$ can more accurately present the clock drift rate of the local nodes in successive time intervals; and the correctness of the correction of the original frequency correction values, which are based on the measured values even/odd doubly periods, is less accurate than $dynratecor1$.

$Error2 = |P_{ji} - P_{ji}'| + |P_{ki} - P_{ki}'| + |P_{li} - P_{li}'|$ is used to detect the clock synchronization performance of node i itself. Besides, it is more often used to conduct nodes' self detection, and it must satisfy the premise that the network is stable, that is to say $Error1 = 0$. If the error is equal to 0, which indicates that the clock synchronization performance of node i could maintain a normal state; if the node is greater than limitpassive2, which signifies that the clock runs abnormally, thus the node should enter the POC: normal passive state; if the node is greater than limithalt2, which indicates that the clock synchronization performance of node i declined obviously, in this condition we should initialize the node. Among them, limitpassive2 and limithalt2 are two threshold values of Error2, and their definition method is similar to Error1, namely

$$limithalt2 = 2 \times pMicroPerMacNom \quad (4)$$

$$limitpassive2 = 0.5 \times limithalt2 \quad (5)$$

The new frequency correction value is

$$dynratecor2 = \text{FTM}(P_{ji}, P_{ki}, P_{li})\qquad(6)$$

With the increase of the number of phase deviation, the clock drift rate and synchronization status information reflected by weight value P will be more accurate. Due to the fact that the dynamic detection method of synchronous node is based on a large number of data acquisitions, the error or loss of individual data will not affect the evaluation and detection results.

4. Interface Design of Hardware of Bus Monitor

BG has its own independent clock synchronization mechanism. This mechanism monitors the TxEN CC (Data Enable Transmit) signals sent out by CC, and through the BGE (Guardian Enable Bus) [10] signal to control the data sent by BD. When CC chooses to send the data in the wrong time slot, BG will notify the host of the error message in an interruption form. Besides, it would disconnect the connection between the node and the network, that is to say, to prohibit the BD continuing to send out data. At the same time, CC would also monitor the BGE signal through BGSM (Guardian Schedule Monitoring Bus) [10]. If the time slot schedule BG obtained functions abnormally, CC will report the error message to the host in an interruption form. Thus, we could define the signal transmission among BG and CC and BD hosts.

BG and the host can be connected through the Peripheral Interface Serial, namely SPI, to achieve configuration function of the host towards BG and send error interruption signal to the host when there is timing error in BG and CC. SPI interface uses the master-slave mode, and this mode is for the synchronous serial data transmission between CPU and peripheral low speed devices. The clock is controlled by the main device. When there is clock shift pulse, the data is transmitted bite by bite. And the high ones are sent earlier, and the lower ones are sent later. The transmission rate of full duplex communication is faster than the I2C bus, reaching up to a several Mbps. According to the connection method between BG and the host and the signal transmission definition, we can get a list of BG hardware interface as shown in table2.

Table 2 Definition of BG interface

BG name	connecting object	BG pin	Input / output	Description
BG (A)	BD (A)	RxD_A	Input	data received by BD (A)
		BGE_A	output	signals controlled by BD (A)(enable / disable)
	CC	$\overline{\text{TxEN\_A}}$	Input	control signal of CC towards BD (A)(enable / disable)
		TBGE_A	output	control signal of BG towards BD (A)(enable / disable)
	host	SCK	Input	clock signal
		SDI	Input	configuration information of BG (A)
		SDO	output	error interrupt information
		$\overline{\text{SCSN}}$	Input	enable signal of BG (A)
BG (B)	BD (B)	RxD_B	Input	the data received of BD (B)
		BGE_B	output	signals controlled by BD (B)(enable / disable)
	CC	$\overline{\text{TxEN\_B}}$	Input	control signal of CC towards BD (B)(enable / disable)
		TBGE_B	output	control signal of BG towards BD (B)(enable / disable)
	host	SCK	Input	clock signal
		SDI	Input	configuration information of BG (B)
		SDO	output	error interrupt information
		$\overline{\text{SCSN}}$	Input	enable signal of BG (B)

The host commands could be divided into two parts, of which one par is the commands sent by host to the CC, and the other part is the commands that the host uses to configure BG, which can be seen in table 8. The third column in the table is the commands sent to the CC, but before the being sent out, we should firstly inform BG of these commands, so that BG could adjust the monitoring strategy in a timely manner; the fourth column in the table is the configuration command of BG.

5. Conclusion

In this paper, we mainly study the FlexRay communication module of wire steering system, and make the communication function of the module could ensure the real-time and fault tolerance of the steer-by-wire system, so as to meet the safety requirements of steer-by-wire design in vehicles.

In terms of scheduling, we out forward two different optimization schemes. Because that, we used scheduling algorithm in the FlexRay static segment, the optimization scheme of this segment is on offline to determine optimal static parameter value and node transmission sequence, in this way to minimize the total response time of all static message. Dynamic segment of FlexRay is based on FTDMA, and this media's access mechanism has time triggering characteristic and is confirmable at the same time. Besides, this media contains the event triggering flexibility. Therefore, to optimize the dispatch of this segment, we must carry on the schedulability analysis based on the worst-case response time of the message to make the optimal scheduling process always meet the prerequisite of system scheduling. And we adopt the optimized scheduling algorithm based on dynamic programming, that is to say, through multi-stage decisions to gradually find the optimal scheduling dynamic segment arrangement. At the same time, we summarize priority solution of the dynamic message.

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